

Introduction

Power considerations in FPGA design are critical for determining the maximum system power requirements and sequencing requirements of the FPGA on the board. This technical note provides users with detailed power considerations such as sequencing. Also included are instructions for calculating power consumption in LatticeECP2™ and LatticeECP2M™ devices using the Power Calculator available in the Lattice ispLEVER® design tool. General guidelines for reducing power consumption are also discussed.

Power Supply Sequencing

Power-Up Sequencing

There are three main power supplies that are required to power-up the LatticeECP2/M device for proper operation: V_{CC} , V_{CCAUX} and V_{CCIO8} . Bank 8, or V_{CCIO8} , powers the sysCONFIG™ port and configuration circuitry and is therefore required during power-up.

The nominal voltages for these power supplies are 1.2V for V_{CC} , 3.3V for V_{CCAUX} and 1.2V to 3.3V for V_{CCIO8} . The nominal trip points for these power supplies are 0.6V to 0.8 V for V_{CC} and V_{CCIO8} , and 2.2V to 2.5V for V_{CCAUX} . For power supply sequencing, refer to the Recommended Operation Conditions section of the [LatticeECP2/M Family Data Sheet](#).

Each power supply must follow a monotonically clean ramp between the trip points and the minimum required supply voltage. Note that for slow ramps (when the power-up ramp rate is 10s or 100s milliseconds) it is critical that the ramp is clean and monotonic. The device may go in and out of the power-up reset if the ramp is unclean and non-monotonic, especially around the trip point. This also applies when powering down the device. A clean, monotonic ramp will ensure that the device will power up and power down properly.

After initialization is complete, if any V_{CC} , V_{CCAUX} or V_{CCIO8} drops below its power-down trip point, the device will reset. Any $V_{CCIO[7:0]}$ can be removed without resetting the device after initialization is complete.

Refer to the [LatticeECP2/M Family Data Sheet](#) and TN1108, [LatticeECP2/M sysCONFIG Usage Guide](#), for configuration timing and power-up information.

Power-Down Sequencing

During power-down, power should be removed from one of the supplies' V_{CC} , V_{CCAUX} or V_{CCIO8} first to ensure that no high currents are seen on the input pins as the other V_{CCIO} supplies are removed. This only applies when input signals are still being driven, such as in hot-socketing applications.

For non-hot-socketing applications, the input signals are likely to be powered from the same supply as V_{CCIO} . Therefore, they will usually be less than or equal to V_{CCIO} during power down.

Power Sequencing Recommendations

LatticeECP2/M devices do not have a power-up sequence requirement. The supplies can be brought up in any sequence.

In order to minimize the transients and hot socketing currents during power up, Lattice recommends that the V_{CC} be brought up before V_{CCAUX} or V_{CCIO8} . Additionally, V_{CC} should reach its minimum voltage value before V_{CCAUX} and V_{CCIO8} reach their minimum values. When removing the supplies, V_{CCAUX} or V_{CCIO8} must be removed before V_{CC} is turned off.

Note that this sequence is not a requirement for LatticeECP2/M devices.

For LatticeECP2MS power-up sequencing, refer to the Recommended Operation Conditions section of the [LatticeECP2/M Family Data Sheet](#).

Power Calculator Hardware Assumptions

The Power Calculator reports the power dissipation in terms of:

1. DC portion of the power consumption
2. AC portion of the power consumption

Total power dissipation is the sum of the static (DC) and dynamic (AC) power dissipations of a device. While DC power depends upon voltage, temperature and process variation, AC power is a strong function of the frequency and the activity of the resources and a weak function of voltage, temperature and process.

Static Power or DC Power

DC power can be further subdivided into the power consumption of the used and unused resources. Another important term is Quiescent Power, the DC power for a blank (BE or Bulk Erase) device. In the Bulk Erase mode, none of the resources are used, so it is the total DC power of an unused device.

The AC portion of the power consumption, associated with used resources, is the dynamic part of the power consumption. AC power dissipation is directly proportional to the frequency and activity at which the resource is running and the number of resource units used.

Junction Temperature

For a fixed temperature, voltage and device package combination, quiescent power is fixed.

Ambient temperature that affects the junction temperature is a factor that contributes to the final power consumption.

Power Calculator models this ambient-to-junction temperature dependency. When a user provides an ambient temperature, it is rolled into an algorithm which calculates the junction temperature and quiescent power through an iterative process.

Typical and Worst Case Process Power/ I_{CC}

Another factor that affects the DC power is process variation. This variation in turn causes variation in quiescent power.

Power Calculator takes these factors into account and allows users to specify either a typical process or a worst case process.

- A typical process selection under Device Variation allows users to calculate the power dissipation of a design using a typical process device.
- The worst case selection under the same option provides the maximum power dissipation for the device and package combination. This information is particularly useful for FPGA power budgeting for the entire system.

Dynamic Power Budgets and Maximum Operating Temperature

When designing a system, designers must make sure a device operates at specified temperatures within the system environment. This is particularly important to consider before a system is designed. With Power Calculator, users can predict device thermodynamics and estimate the dynamic power budget. The ability to estimate a device's operating temperature prior to board design also allows the designer to better plan for power budgeting and airflow.

Although total power, ambient temperature, thermal resistance and airflow all contribute to device thermodynamics, the junction temperature (as specified in the device data sheet) is the key to device operation. The allowed junction temperature range is 0°C to 85°C for commercial devices and -40°C to 100°C for industrial devices. Any time the junction temperature of the die falls out of these ranges, the performance and reliability of the device's operation

must be evaluated. The reliability limit of junction temperature, on the other hand, for this generation of device technology is 125°C.

Let us consider an example for how to determine and use the Power Calculator for thermal analysis. Once the user has imported or provided all the required information in the Power Calculator, the software will provide the power estimation and predict the Junction Temperature (T_J). Any time this junction temperature is outside the limits specified in the device data sheet, the viability of operating the device at this junction temperature must be re-evaluated. A commercial device is likely to show speed degradation with a junction temperature above 85°C and an industrial device at a junction temperature will degrade above 100°C. It is required that the die temperature be kept below these limits to achieve the guaranteed speed operation.

Operating a device at a higher temperature also means a higher SICC. The difference between the SICC and the total ICC (both Static ICC and Dynamic ICC) at a given temperature provides the dynamic budget available. If the device runs at a dynamic ICC higher than this budget, the total ICC is also higher. This causes the die temperature to rise above the specified operating conditions.

There are a number of ways to handle this situation. Some of these are discussed in the Power Management section of this document. The four factors listed earlier in this section, namely power, ambient temperature, thermal resistance and airflow, can also be varied and controlled to reduce the junction temperature of the device.

Power Calculator is a powerful tool to help system designers properly budget the FPGA power that in turn helps improve the overall system reliability.

Power Calculator

Power Calculator is a powerful tool that allows users to estimate power consumption at two different levels:

1. Estimate of the utilized resources before completing place and route
2. Post place and route design

At a coarse level of estimation, the user provides estimates of device usage in the Power Calculator Wizard and the tool provides a rough estimate of the power consumption.

For a more accurate approach, a designer can import actual device utilization by importing the post Place and Route netlist (NCD) file.

Power Calculation Equations

The following are the power equations used in the Power Calculator:

$$\begin{aligned} \text{Total DC Power (Resource)} &= \text{Total DC Power of Used Portion} + \text{Total DC Power of Unused Portion} \\ &= [\text{DC Leakage per Resource when Used} * N_{\text{RESOURCE}}] \\ &\quad + [\text{DC Leakage per Resource when Unused} * (N_{\text{TOTAL RESOURCE}} - N_{\text{RESOURCE}})] \end{aligned}$$

Where:

$N_{\text{TOTAL RESOURCE}}$ is the total number of Resources in a device.

N_{RESOURCE} is the number of Resources used in the design.

The total DC power consumption for all the resources as per the design data is the sum of the quiescent power and the individual DC power of the resources in the Power Calculator.

$$\begin{aligned} \text{Total DC Power (I}_{\text{CCAUX}}\text{)} &= K_{\text{RESOURCE}} * 525 \mu\text{A} + \text{Typical Standby I}_{\text{CCAUX}} \end{aligned}$$

Where:

$K_{RESOURCE}$ is the number of reference input I/O such as HSTL/SSTL. For LVDS $K_{RESOURCE}$ is number of inputs divided by two.

I_{CCAUX} is a DC current that does not change with I/O toggle rate or temperature.

Typical Standby I_{CCAUX} is found in the data sheet.

The AC power, on the other hand, is governed by the following equation:

$$\begin{aligned} \text{Total AC Power (Resource)} \\ = K_{RESOURCE} * f_{MAX} * AF_{RESOURCE} * N_{RESOURCE} \end{aligned}$$

Where:

$N_{RESOURCE}$ is the number of resources used in the design.
 $K_{RESOURCE}$ is the power constant for the resource in mW/MHz.
 f_{MAX} is the max. frequency at which the resource is running. Frequency is measured in MHz.
 $AF_{RESOURCE}$ is the activity factor for the resource group. The Activity Factor is a percentage of the switching frequency.

For example, the power consumption of the LUT is calculated as per the following equation,

$$\begin{aligned} \text{Total AC Power (LUT)} \\ = K_{LUT} * f_{MAX} * AF_{LUT} * N_{LUT} \end{aligned}$$

Where:

N_{LUT} is the number of LUTs used in the design.
 K_{LUT} is the Power constant for the LUT blocks in mW/MHz.
 f_{MAX} is the max. frequency of the LUT clock measured in MHz.
 AF_{LUT} is the activity factor for the LUT. The Activity Factor is a percentage of the switching frequency.

Another example is the power consumption of the EBR block, which is calculated as follows:

$$\begin{aligned} \text{Total AC Power (EBR)} \\ = K_{EBR} * f_{MAX} * AF_{EBR} * N_{EBR} \end{aligned}$$

Where:

N_{EBR} is the number of EBR blocks used in the design.
 K_{EBR} is the power constant for the EBR blocks in mW/MHz.
 F_{MAX} is the max. frequency of the EBR clock measured in MHz.
 AF_{EBR} is the activity factor for the Read and Write ports of the EBR. The Activity Factor is a percentage of the switching frequency.

Also note that the LUT can be configured in Logic, Ripple or Distributed RAM modes. Each of these modes has a different power constant/power coefficient. However, the equations stay the same.

The AC power of some of the dedicated blocks can be calculated using the following equation:

$$\begin{aligned} \text{Total AC Power (Dedicated Resource)} \\ = K_{RESOURCE} * f_{MAX} * N_{RESOURCE} \end{aligned}$$

Where:

$N_{RESOURCE}$ is the number of resources used in the design.
 $K_{RESOURCE}$ is the power constant for the resource in mW/MHz.
 f_{MAX} is the max. frequency at which the resource is running measured in MHz.

Activity Factor Calculation

The Activity Factor % (or AF%) is defined as the percentage of frequency (or time) that a signal is active or toggling the output.

Most resources associated with a clock domain are running or toggling at some percentage of the frequency at which the clock is running. Users must provide this value as a percentage under the AF% column in the Power Calculator tool.

Another term for I/Os is the I/O Toggle Rate. The AF% is applicable to the PFU, Routing, and Memory Read Write Ports, etc. The activity of I/Os is determined by the signals provided by the user (in the case of inputs) or as an output of the design (in the case of outputs). The rates at which I/Os toggle define their activity. The I/O Toggle Rate or the I/O Toggle Frequency is a better measure of their activity.

The Toggle Rate (or TR) in MHz of the output is defined in the following equation:

$$\text{Toggle Rate (MHz)} = 1/2 * f_{\text{MAX}} * \text{AF\%}$$

Users are required to provide the TR (MHz) value for the I/O instead of providing the frequency and AF% for other resources.

AF can be calculated for each routing resource, output or PFU. However, this involves long calculations. The general recommendation for a design occupying roughly 30% to 70% of the device is an AF% between 15% and 25%. This is an average value. The accurate value of an AF depends upon clock frequency, stimulus to the design and the final output.

Ambient and Junction Temperatures and Airflow

A common method of characterizing a packaged device's thermal performance is with Thermal Resistance, θ . In a semiconductor device, thermal resistance indicates the steady state temperature rise of the die junction above a given reference for each watt of power (heat) dissipated at the die surface. Its units are °C/W.

The most common examples are θ_{JA} , Thermal Resistance Junction-to-Ambient (in °C/W) and θ_{JC} , Thermal Resistance Junction-to-Case (also in °C/W). Another factor is θ_{JB} , Thermal Resistance Junction-to-Board (in °C/W).

Knowing the reference (i.e. ambient, case or board) temperature, the power and the relevant θ value, the junction temperature can be calculated as follows.

$$T_J = T_A + \theta_{JA} * P \quad (1)$$

$$T_J = T_C + \theta_{JC} * P \quad (2)$$

$$T_J = T_B + \theta_{JB} * P \quad (3)$$

Where T_J , T_A , T_C and T_B are the Junction, Ambient, Case (or Package) and Board temperatures (in °C) respectively. P is the total power dissipation of the device.

θ_{JA} is commonly used with natural and forced convection air-cooled systems. θ_{JC} is useful when the package has a high conductivity case mounted directly to a PCB or heat sink. θ_{JB} applies when the board temperature adjacent to the package is known.

Power Calculator utilizes the ambient temperature (°C) to calculate the junction temperature (°C) based on the θ_{JA} for the targeted device, per equation 1 above. Users can also provide the airflow values (in LFM) to get a more accurate value of the junction temperature.

Managing Power Consumption

One of the most critical factors in design today is reducing the system power consumption. Low power consumption is especially important for hand-held devices and other modern electronic products. There are several design techniques that can significantly reduce overall system power consumption. These include:

1. Reducing the operating voltage.
2. Operating within the specified package temperature limitations.
3. Using optimum clock frequency to reduce power consumption, as the dynamic power is directly proportional to the frequency of operation. Designers must determine if a portion of their design can be clocked at a lower rate, which will reduce power.
4. Reducing the span of the design across the device. A more closely placed design utilizes fewer routing resources for less power consumption.
5. Reducing the voltage swing of the I/Os where possible.
6. Using optimum encoding where possible. For example, a 16-bit binary counter has, on average, only 12% Activity Factor and a 7-bit binary counter has an average of 28% Activity Factor. On the other hand, a 7-bit Linear Feedback Shift Register can toggle as much as 50% Activity Factor, which causes higher power consumption. A gray code counter, where only one bit changes at each clock edge, will use the least amount of power, as the Activity Factor is less than 10%.
7. Minimizing the operating temperature, by the following methods:
 - a. Use packages that can better dissipate heat. For example, packages with lower thermal impedance.
 - b. Place heat sinks and thermal planes around the device on the PCB.
 - c. Better airflow techniques using mechanical airflow guides and fans (both system fans and device-mounted fans).

Power Calculator Assumptions

The following are the assumptions made by the Power Calculator:

1. The Power Calculator tool uses equations with constants based on a room temperature of 25°C.
2. The user can define the Ambient Temperature (T_A) for device Junction Temperature (T_J) calculation based on the power estimation. T_J is calculated from the user-entered T_A and the power calculation of typical room temperature.
3. I/O power consumption is based on an output loading of 5pF. Users have the ability to change this capacitive loading.
4. Users can estimate power dissipation and current for each type of power supplies that are V_{CC} , V_{CCIO} , V_{CCJ} , and V_{CCAUX} . For V_{CCAUX} , only static I_{CCAUX} values are provided in the Power Calculator.
Additional V_{CCAUX} contributions due to differential output buffers, differential input buffers and reference input buffers must be added per pair for differential buffers or per pin for reference input buffers according to the user's design. See the equation given in this technical note for Total DC Power (I_{CCAUX}).
5. The nominal V_{CC} is used by default to calculate the power consumption. A lower or higher V_{CC} can be chosen from a list of available values.
6. Users can enter an Airflow in Linear Feet per Minute (LFM) along with a Heat Sink option to calculate the Junction Temperature.
7. The default value of the I/O types for the LatticeECP2/M devices is LVCMOS12, 6mA.
8. The Activity Factor is defined as the toggle rate of the registered output. For example, assuming that the input of a flip-flop is changing at every clock cycle, 100% AF of a flip-flop running at 100MHz is 50MHz.

Technical Support Assistance

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Revision History

| Date | Version | Change Summary |
|----------------|---------|--|
| February 2006 | 01.0 | Initial release. |
| September 2006 | 01.1 | Updated for LatticeECP2/M. |
| | | Added discussion on Dynamic Power Budgets and Junction Temperature. |
| November 2006 | 01.2 | Added calculation of I_{CCAUX} in Power Calculation Equations section. |
| January 2007 | 01.3 | Updated Power Supply Sequencing section. |
| November 2009 | 01.4 | Updated Power-up Sequencing text section. |
| | | Updated Power Sequencing Recommendations text section. |
| June 2013 | 01.5 | Updated document with new corporate logo. |
| | | Updated Technical Support Assistance information. |