

## Introduction

Every new technology becomes legacy technology at some point in its life. Most systems contain a combination of new and old technologies. Current legacy technologies include computer buses, interfaces, peripheral devices, and I/O ports that were designed in the earlier era of industry standards, and which have not evolved sufficiently to take advantage of the capabilities of today's more manageable, faster, and far more efficient architectures.

Reducing the impact of legacy technologies on current system architectures and retaining backward compatibility is a goal in every design. These problems are solved through the flexibility of LatticeSC™ PURESPEED™ I/O interfaces, which have been designed to meet the demanding requirements of today's designs and maintaining the needs of older standards.

Each PURESPEED I/O buffer can be programmable to support single-ended and differential I/O standards. Some of the single-ended standards are LVCMOS, LVTTTL, SSTL, HSTL, PCI, GTL, GTLP, AGPIX and AGP2X. Most of these buffers are supported directly around the entire device. However for direct support of 3.3V I/O types could be bounded by physical location. Using the flexibility of the LatticeSC 2.5V voltage-referenced I/O buffers can solve this physical limitation and meet the performance of legacy buses.

The application note will discuss and detail the solution of using the 2.5V PURESPEED I/O solution to interface to 3.3V standard legacy I/O designs.

## Usage Details

For 3.3V legacy systems requiring fairly high drive capability, a large number of I/Os, and line impedances down to about 25 ohms, the LatticeSC offers 3.3V I/O banks that directly support these standards at speeds of 200MHz or less. These standard 3.3V LVTTTL/LVCMOS I/O are typically defined with DC interface parameters for digital circuits operating from a 3.0V or 3.3V power supply and driving or being driven by LVTTTL/LVCMOS-compatible devices. The 3.3V LVTTTL/LVCMOS standards are general-purpose, single-ended standards used for 3.3V applications. This I/O standard does not require input reference voltages ( $V_{REF}$ ) or termination voltages ( $V_{TT}$ ). These I/O standards are directly supported in VCCIO banks 1, 4, and 5 of the LatticeSC architecture.

The LatticeSC can maximize device I/O utilization for 3.3V interfaces by taking advantage of 2.5V I/O banks. This is accomplished by using the enhanced transceiver logic features of SSTL25 buffers while maintaining compatible TTL/CMOS output switching levels. The features of these single-ended I/O permit voltage scalable options by taking advantage of the integrated terminations and work well in point to point interconnections.

As shown in Figure 1, the LatticeSC is interfaced to a 3.3V CMOS device using a SSTL25 I/O in a 2.5V VCCIO bank. The LatticeSC implementation uses the 60-ohm dynamic termination (DDRII type) to a  $V_{TT}$  termination voltage of  $1.25V \pm 5\%$ . The 60-ohm dynamic termination ( $R_T$ ) places the termination in-circuit when receiving and is off when driving. The range of  $V_{TT}$  can vary between 1.19 and 1.31V across the devices PVT deviations.  $R_T$  is nominal 60-ohm  $\pm 20\%$  or 48 to 72-ohm.

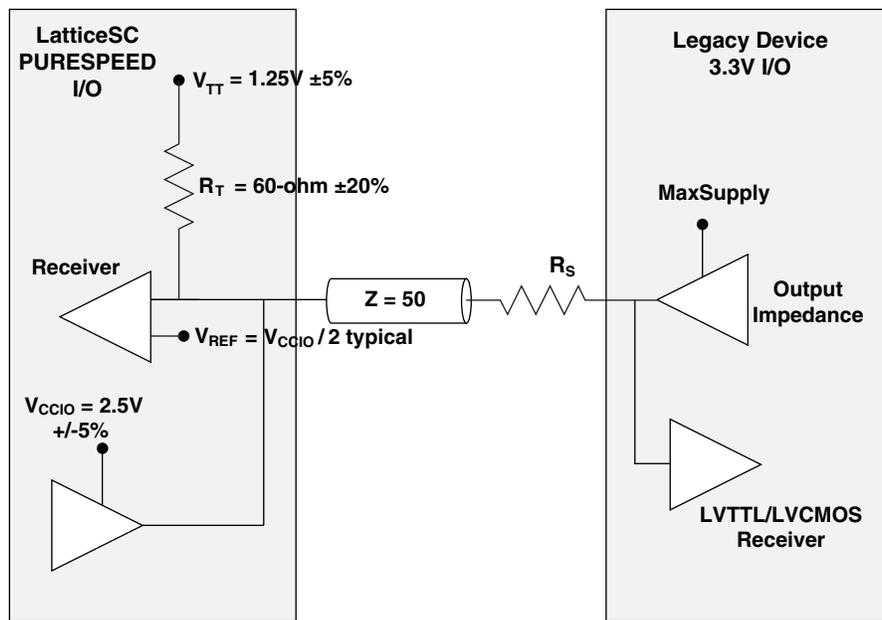
In the most common scenario, a unidirectional bus between the LatticeSC device and a legacy CMOS device is easily completed. This case includes a LatticeSC receiver with a constant  $V_{TT}$  termination or an external termination resistor. The  $V_{TT}$  connected resistor reduces the input  $V_{IH}$  on the low-voltage input.  $V_{IH}$  can also be reduced using a series resistor on the CMOS output driver. The  $V_{IH}$  is reduced via the voltage divider of  $R_T$  and the output driver or  $R_T$  and  $R_S$ . LatticeSC outputs will drive directly without termination. A careful calculation of the minimum line impedance using Lattice supplied IBIS models needs to be completed to ensure the output driver strength is set accordingly as to not over drive the LatticeSC input buffer beyond the values shown in the LatticeSC Family Data Sheet.

Bidirectional busses are possible using careful design criteria. The bus turnaround time for bidirectional switching must be handled properly.  $V_{TT}$  must be activated before the legacy device begin's driving. The dynamic  $V_{TT}$  should be turned off before LatticeSC begins driving. This scenario must include a cycle of bus latency for the  $V_{TT}$  switches. The legacy device may also include an external resistor on the output driver to limit the  $V_{IH}$  on the LatticeSC device input buffer. The net effect of the voltage applied is that the input pin on the LatticeSC device cannot exceed 2.74V as a DC level. See the LatticeSC Family Data Sheet for specifications of both maximum  $V_{IH}$  levels allowed for both DC and AC (i.e. overshoot) operation.

This implementation uses  $V_{TT}$  pins that are standard with any LatticeSC HSTL and SSTL I/O types. More detailed information can be found in Lattice technical note number TN1088, *LatticeSC PURESPEED I/O Usage Guide*.

The LatticeSC SSTL output characteristics meet all the DC parameters for a typical 3.3V TTL bus. The LatticeSC input buffer characteristics need to be carefully analyzed as the device has a maximum allowable pad voltage of 2.74V and a maximum pad current of 30mA.

Figure 1. SSTL25 to Legacy Device 3.3V Bidirectional Interface



Designers can analyze the proposed solution by solving the  $V_{MAX}$  and  $I_{MAX}$  that will be asserted on the LatticeSC input Figure 1.

$$PADV_{MAX} = V_{TT_{MAX}} + (Legacy\ MaxSupply - V_{TT_{MAX}}) * R_T / (R_{T_{MAX}} + R_{S_{MIN}} + Legacy\ MinImpedance)$$

$$I_{MAX} = PADV_{MAX} - V_{TT_{MAX}} / R_{T_{MAX}}$$

The maximum voltage on the pad cannot exceed the data sheet specified maximum Input ( $V_{IH}$ ) or I/O Tristate Voltage Applied (Banks 2, 3, 6, 7) of 2.74V on the LatticeSC device. Therefore, this implementation will allow for the use of 2.5V I/O banks to be used in the 3.3V interface application.

Shown below is an example software preference for an SSTL25 application used as a 3.3V bus interface.

```
##### Pin Group for Legacy bidi bus
DEFINE PORT GROUP "legacy_bidi"
##### bidi bus IO Rules to interface to 3.3V bus
IOBUF GROUP "legacy_bidi" IO_TYPE=SSTL25_I TERMINATEVTT=60 IMPEDANCE=33
VCMT=DDR_II SLEWRATE=SLOW ;
##### Locate pins in VCCIO Bank 5
```

```
LOCATE COMP "PIO_0" SITE "AJ4" ;
LOCATE COMP "PIO_1" SITE "AE11" ;
LOCATE COMP "PIO_2" SITE "AF10" ;
LOCATE COMP "PIO_3" SITE "AH7" ;
LOCATE COMP "PIO_4" SITE "AH8" ;
LOCATE COMP "PIO_5" SITE "AE12" ;
LOCATE COMP "PIO_6" SITE "AE13" ;
LOCATE COMP "PIO_7" SITE "AK4" ;
```

Note: For LatticeSC device/package combinations that do not include VTT I/O, the circuitry in Figure 1 must be implemented external to the device.

## Conclusion

The physical limitations of the LatticeSC I/O banks are specified as guidelines to the FPGA designer. The typical scenarios for FPGA designs are usually straightforward and are accomplished utilizing the standard LatticeSC design flow. However a complete understanding of the flexible I/O features of the LatticeSC often offers a solution to legacy interfaces and maximizes the utilization of the FPGA.

## References

- LatticeSC Family Data Sheet
- Lattice Technical Note TN1088, *LatticeSC PURESPEED I/O Usage Guide*
- ispLEVER® Software Documentation

## Technical Support Assistance

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## Revision History

Date	Version	Change Summary
November 2006	01.0	Initial release.