

## Introduction

This technical note describes a physical layer 10 Gigabit Ethernet XAUI (10 Gbps) interoperability test between a LatticeECP2M™ FPGA and the Marvell Alaska 88X2040 device. The test was limited to the physical layer (up to XGMII) of the 10-Gigabit Ethernet protocol stack.

Specifically, this document discusses the following topics:

- Overview of LatticeECP2M devices and Marvell Alaska 88X2040 devices
- \* XAUI physical layer interoperability setup, testing, and results

## XAUI Interoperability

XAUI is a high-speed interconnect that offers reduced pin count and the ability to drive up to 20" of PCB trace on standard FR-4 material. In order to connect a 10-Gigabit Ethernet MAC to an off-chip PHY device, an XGMII interface is used. The XGMII is a low-speed parallel interface for short range (approximately 2") interconnects.

XAUI interoperability is based on the 10-Gigabit Ethernet standard (IEEE Standard 802.3ae-2002). Two XAUI link partners can be directly plugged into a XAUI backplane. Both boards are capable of generating and checking packets.

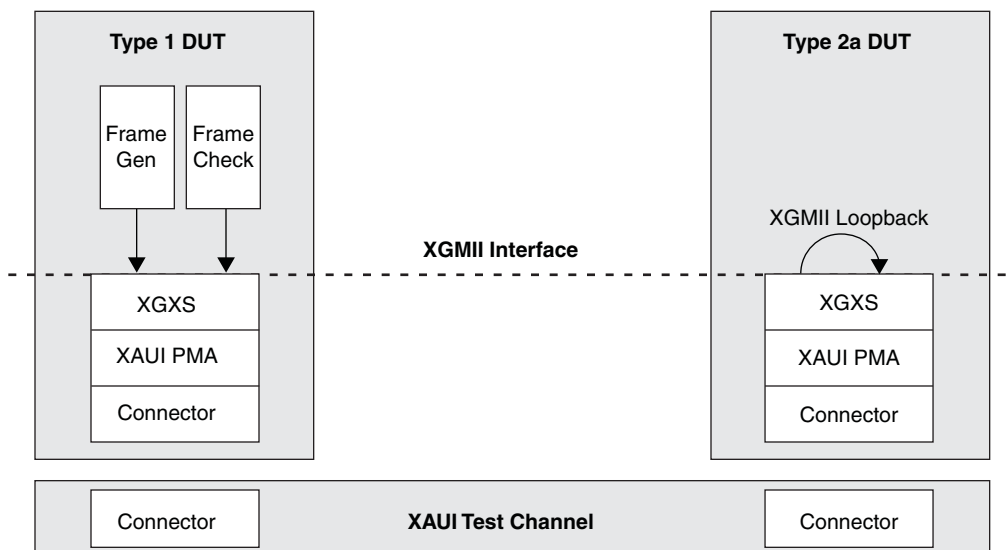
The board that sources packets is capable of keeping a detailed count of the number of packets transmitted while the sink board is capable of keeping detailed statistics on the number of packets received and errors associated with the packets. The XAUI backplane is also called the XAUI test channel. A typical test setup is shown in Figure 1.

Each reference station must be a line card that is directly plugged into the XAUI test channel. Both DUTs are required to have their own clock domain. Synchronous clocking (distributing a single clock to the two DUTs) is not allowed. Local management indicators on the DUT (reference stations) that provide information on link level errors such as CRC errors are also needed. A DUT is called a Type #1 device if it is capable of transmitting and checking packets.

A DUT is called a Type #2a device if it receives packets and does a RX-to-TX loopback through XGMII and sends the packets back to the transmitting station, which is a Type #1 device. The Type #1 device then checks the received packets for errors. Figure 1 shows a setup where one DUT is of Type #1 and the other is of Type #2a.

The LatticeECP2M and Marvell Alaska 88X2040 interoperability exercises the whole physical layer, including XGMII.

Figure 1. Typical XAUI Interoperability Test Setup



## LatticeECP2M Overview

The LatticeECP2M family is the industry's only true low-cost FPGA family with built-in SERDES. This family of devices includes features to meet the needs of today's communication network systems.

The LatticeECP2M family also feature up to 16 channels of embedded SERDES with associated Physical Coding Sublayer (PCS) logic. The PCS logic can be configured to support numerous industry standard high-speed data transfer protocols.

### LatticeECP2M in XAUI Mode

The LatticeECP2M XAUI IP was used for the interoperability exercise. The LatticeECP2M SERDES/PCS in XAUI mode along with the Lattice XAUI IP provide full compatibility from Serial I/O to the XGMII interface of the IEEE 802.3-2002 XAUI standard.

#### Transmit Path Functionality (From LatticeECP2M Device to Line)

- Transmit State Machine which performs translation of XGMII idles to proper ||A||, ||K||, ||R|| characters according to the IEEE 802.3ae-2002 specification
- 8b10b encoding

#### Receive Path Functionality (From Line to LatticeECP2M Device)

- Word alignment based on IEEE 802.3-2002-defined alignment characters
- 8b10b decoding
- Link State Machine functions incorporating operations defined in the PCS Synchronization State Diagram of the IEEE 802.3ae-2002 specification
- Clock Tolerance Compensation logic capable of accommodating clock domain differences
- Receive State Machine compliant to the IEEE 802ae.3-2002 specification

## Marvell Alaska 88X2040 Overview

The Marvell 88X2040 Quad transceiver is a fully integrated serialization/de-serialization device that incorporates four independent lanes, delivering high-speed bi-directional point-to-point baseband data transmission that supports cost-effective IEEE 802.3ae compliant 10-Gigabit Ethernet and 10-Gigabit Fibre Channel applications.

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The 88X2040 Quad can be configured either as four separate high-speed lanes or as a single data path with four synchronized lanes. It supports a wide range of serial data rates from 1.0 Gbps to 3.1875 Gbps. The 88X2040 supports the 32-bit bi-directional 10-Gigabit Media Independent Interface (XGMII) with 8b10b ENDEC option, and the extended Auxiliary Unit Interface (XAUI). The 88X2040 performs the parallel-to-serial, serial-to-parallel conversion with integrated Time Base Generator (TBG) and Clock/Data Recovery Circuit (CDRC).

On-chip synthesis performed by the high performance, high frequency, and low jitter phase-locked loop on the 88X2040 transceiver allows the use of cost-effective, low frequency clock references. On-chip clock synthesis is performed to meet compliance with the bit error rate (BER) requirement of associated ANSI, Bellcore, and ITU-T standards.

The 88X2040 supports pre-emphasis on the serial driver to compensate for losses in a copper environment.

Marvell Alaska 88X2040 features:

- IEEE 802.3ae/10GFC compliant Quad 3.125 Gbps/lane transceiver
- Supports IEEE 802.3ae/10GFC XGMII parallel interface
- Supports IEEE 802.3ae/10GFC XAUI serial interface
- Allows maximum 20 Gbps full-duplex data throughput
- On-chip 8b10b Encoding/Decoding (ENDEC)
- On-chip Time Base Generator
- Elastic buffering
- Supports pre-emphasis on the serial driver
- On-chip 50-ohm serial receiver termination
- IEEE 1149.1 JTAG test interface
- 1.5V, 3.3V, and 1.8V power supplies
- 1.5V or 1.8V HSTL I/O
- Selectable 62.5 MHz, 125 MHz, or 156.25/159.375 MHz reference clock input
- Exceeds IEEE 802.3ae jitter requirement
- Advance 0.15  $\mu$ m digital CMOS process.

## **Test Equipment**

The equipment used in the interoperability test is described below.

### **Marvell 88X2040 SMA-to-XGMII Evaluation Board**

The 88X2040 is a quad 3.125 Gbps transceiver which serializes XGMII signals and de-serializes XAUI signals. On the 88X2040 board, the XGMII signals are looped back from the receive side to the transmit side and the XAUI signals are connected to SMA connectors. This evaluation board is designed to use the internal packet generator and receive packet counters to evaluate the transceiver.

The board includes:

- The capability to use an on-board 156.25 MHz oscillator clock source or an external source from an SMA input
- MDIO/MDC monitoring/control to both devices
- Eight Transmit SMAs and eight Receive SMAs for access to the 88X2040 SERDES.

### **Marvell Alaska X 88X2040 Software**

The Alaska X 88X2040 software GUI controls the 88X2040 devices and monitors status bits through MDIO/MDC.

The GUI is sub-divided into several sections.

**Rate and Pattern Section**

- The reference clock is set to 156.25 MHz
- Speed is set to 3.125 Gbps (XAUI rate per channel)
- Either CJPAT or CRPAT can be selected for test pattern

**Pattern Generator Section**

- Selecting the TX button transmits the above selected pattern to the SERDES outputs. The Packet Transmitted counter keeps track of the number of packets transmitted.
- De-selecting the TX button puts the 88X2040 board in external loopback mode. In this mode, the pattern at the XGMII RX side is looped back to the XGMII TX side and sent to the SERDES SMA outputs.
- Selecting the RX enables the RX counters to count the number and rate of Good and Error received packets (of the selected pattern).

**Pre-Emphasis and Amplitude Control Section**

This section provides amplitude and pre-emphasis control for all four XAUI SERDES channels.

**Link Status Section**

This section provides information on the status of the XAUI link. For proper linking, the individual Lane Sync indicators for all four channels, as well as the Aligned and Link indicators should all be green.

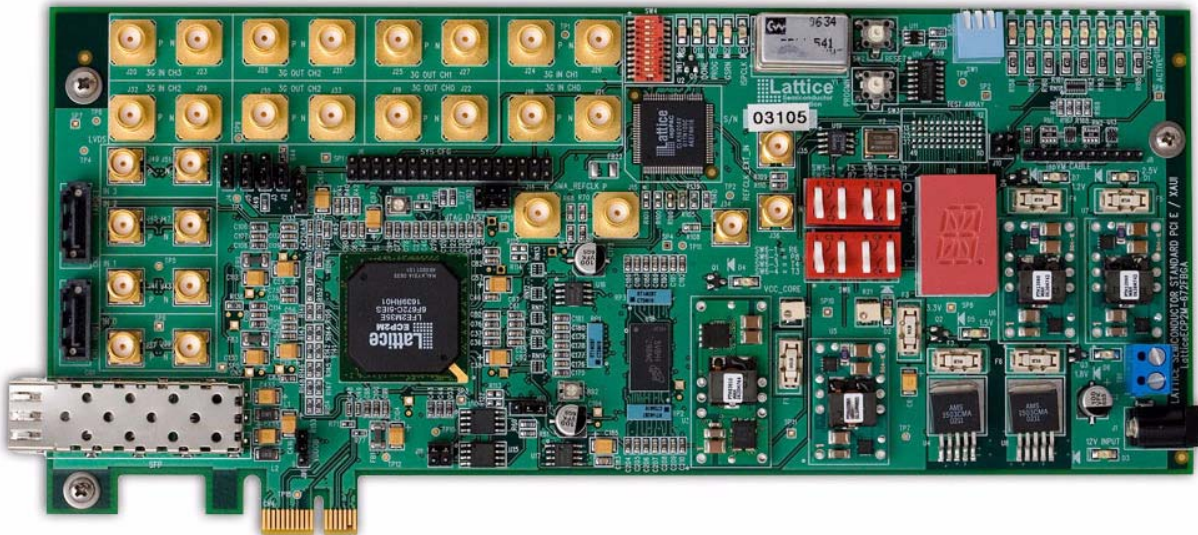
**LatticeECP2M SERDES Evaluation Board**

The LatticeECP2M SERDES Evaluation Board provides a stable yet flexible platform designed to help the user quickly evaluate the performance of the LatticeECP2M SERDES and FPGA, or aid in the development of custom designs.

The LatticeECP2M SERDES Evaluation Board features:

- An LFE2M50E-6F672C FPGA device
- SMA connectors for SERDES I/O, LVDS evaluation, and external clock I/O
- x1 PCI Express edge connector (*Note: Only available with LatticeECP2M-50 or larger FPGA installed*)
- On-board DDR2 memory
- SFP transceiver cage and associated interface (*Note: Only available with LatticeECP2M-50 or larger FPGA installed*)
- SATA-like connections to SERDES channels (*Note: Only available with LatticeECP2M-50 or larger FPGA installed*)
- On-board Flash configuration memory
- Various LEDs, switches, connectors, I/O headers, high-speed layout structures, and on-board power control.

Figure 2 shows the LatticeECP2M SERDES Evaluation Board.

**Figure 2. LatticeECP2M SERDES Evaluation Board**

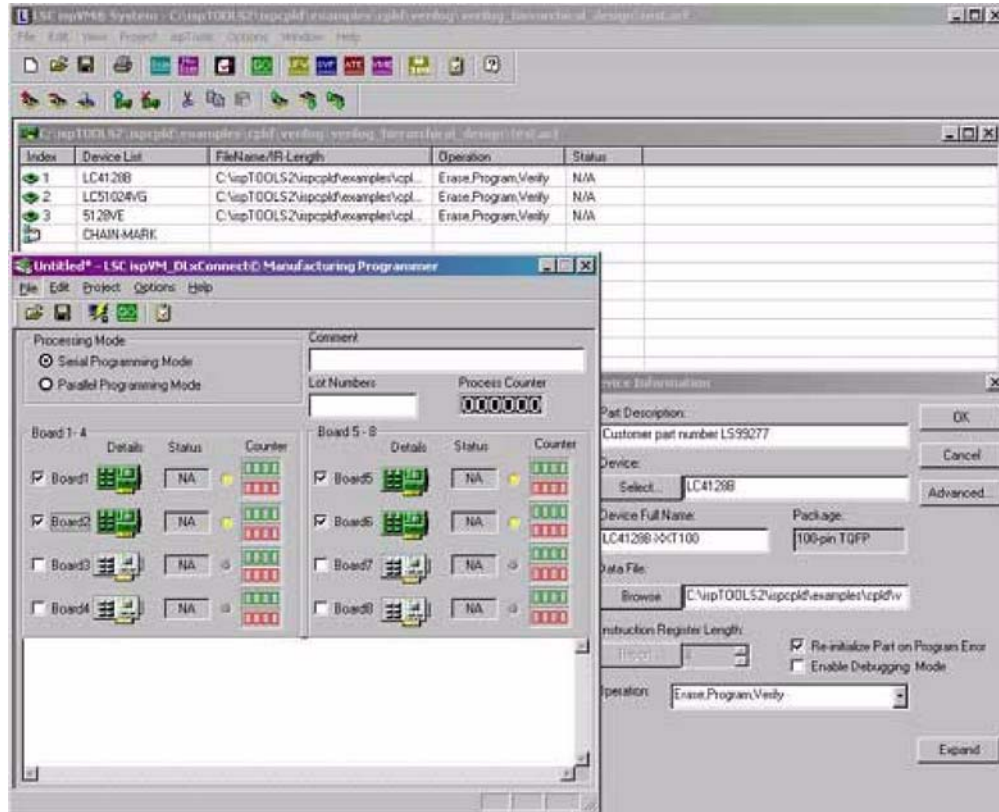
### ispVM™ System Software

The ispVM System is included with Lattice's ispLEVER® software, and is also available as a stand-alone device programming manager. The ispVM System is a comprehensive design download package that provides an efficient method of programming ISP devices using JEDEC and Bitstream files generated by Lattice Semiconductor, and other, design tools. This complete device programming tool allows the user to quickly and easily download designs through an ispSTREAM to devices and includes features that facilitate ispATE™, ispTEST, and ispSVF programming as well as gang-programming with DLxConnect.

The ispVM System is used in this interoperability test to download the LatticeECP2M bitstream, which configures the device in 10-Gigabit Ethernet mode (XAUI).

Figure 3 shows a screen shot of the ispVM System software.

Figure 3. ispVM System Software Screen Shot



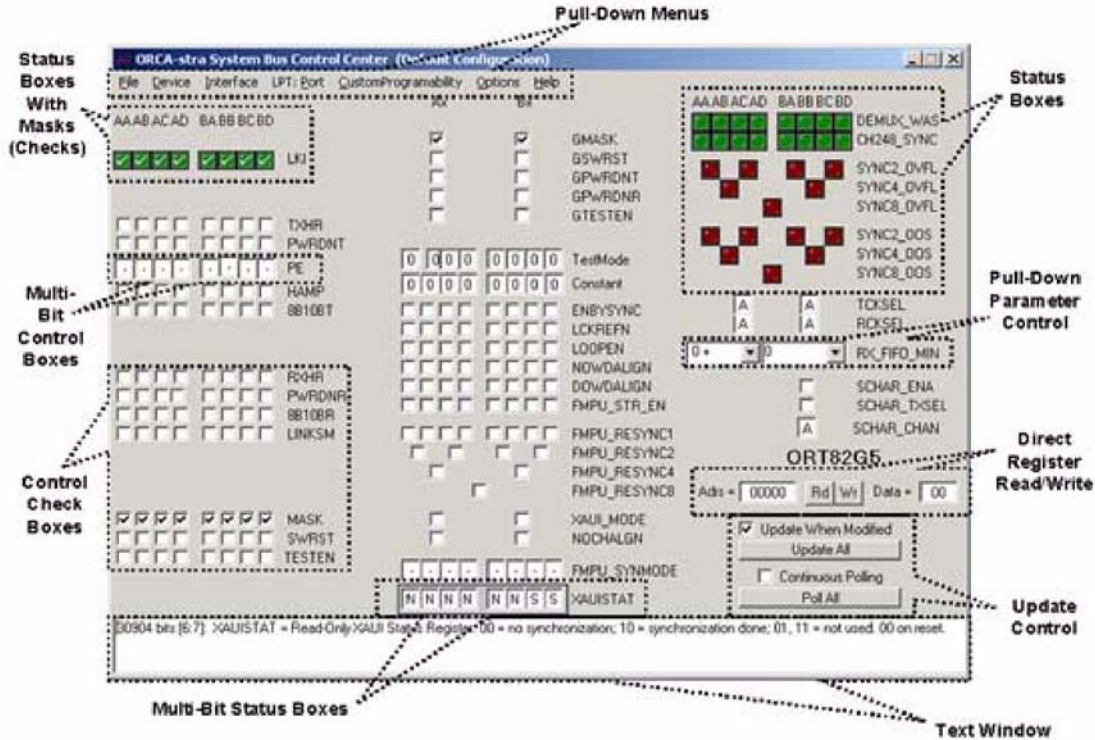
### ORCAstra System Software

The Lattice ORCAstra software is a PC-based graphical user interface that allows the user to configure the operational mode of an FPGA by programming control bits in the on-chip registers. This helps users quickly explore configuration options without going through a lengthy re-compile process or making changes to their board.

Configurations created in the GUI can be saved to memory and re-loaded for later use. A macro capability is also available to support script-based configuration and testing. The GUI can also be used to display system status information in real time. Use of the ORCAstra software does not interfere with the programming of the FPGA portion of the LatticeECP2M.

Figure 4 is a screen shot of the ORCAstra System software.

Figure 4. ORCAstra System Software Screen Shot



## Interoperability Testing

This section provides details on the XAUI interoperability test between the LatticeECP2M device and the Marvell 88X2040 device. The purpose of the test is to implement interoperability between one Type #1 DUT (88X2040) and one Type #2 DUT (LatticeECP2M).

The test has the following characteristics:

- Independent (asynchronous) +/- 100 ppm clock sources clock the LatticeECP2M and 88X2040 devices. For these particular devices, the data rate across four lanes is  $4 \cdot 8/10 \cdot 20 \cdot F$ , where F is the source clock frequency. The data rate in XAUI mode is 10 Gbps. This means an independent clock source of 156.25 MHz (+/- 100 ppm) or larger clocks each device.
- The 88X2040 device transmits CJPAT data to the LatticeECP2M device
- The LatticeECP2M device loops the data at its XGMII interface back to the 88X2040 device

By the end of the test:

- The LatticeECP2M device RX ERR counters should remain at zero
- The LatticeECP2M device visual window counters should report as many TX packets generated as RX packets received
- The amount of test time should be longer than 30 minutes to ensure the error rate is less than 10-12 with 99.999999% accuracy

## Test Setup

The setup includes:

- A Tyco Backplane (using the 16" HM-ZD slots)
- Marvell 88X2040 evaluation LB SMA board (with the 88X2040 devices)

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- LatticeECP2M SERDES Evaluation Board
- One SMA to HM-ZD daughter card to go from the Marvell SMA connections to the Tyco HM-ZD slot
- One SMA to HM-ZD daughter card to go from the LatticeECP2M SMA connections to the Tyco HM-ZD slot
- A PC for software control/monitoring
- One 156.25 MHZ differential clock box to provide an external reference clock to the LatticeECP2M SERDES Evaluation Board. The Marvell 88X2040 board contains a built-in oscillator.
- About 12" of SMA cable to connect the Marvell board to its daughter card
- About 12" of SMA cable to connect the LatticeECP2M SERDES Evaluation Board to its daughter card

Figure 5 is a block diagram of the test setup.

Figure 6 shows the Marvell 88X2040 board, the LatticeECP2M SERDES Evaluation Board, and the TYCO back-plane connections.

***Figure 5. Board Connections***

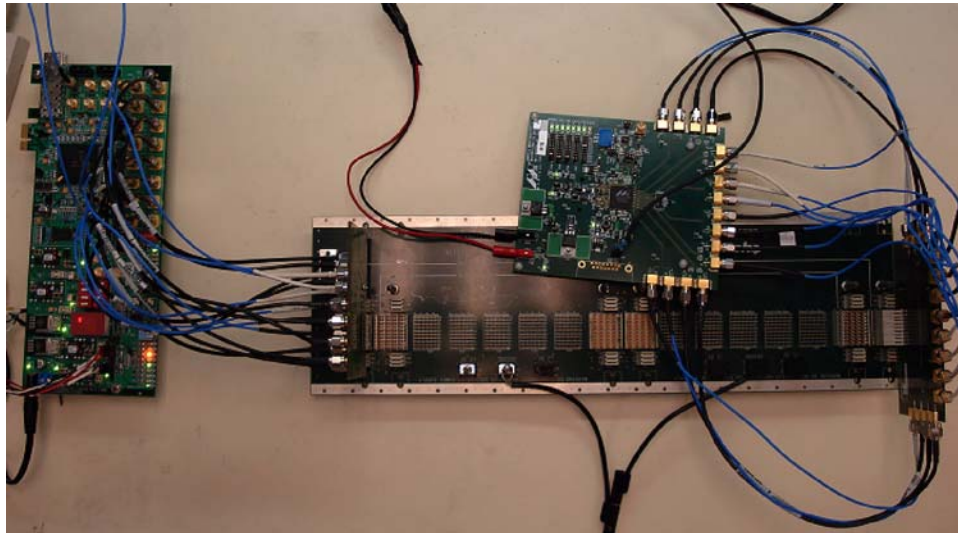
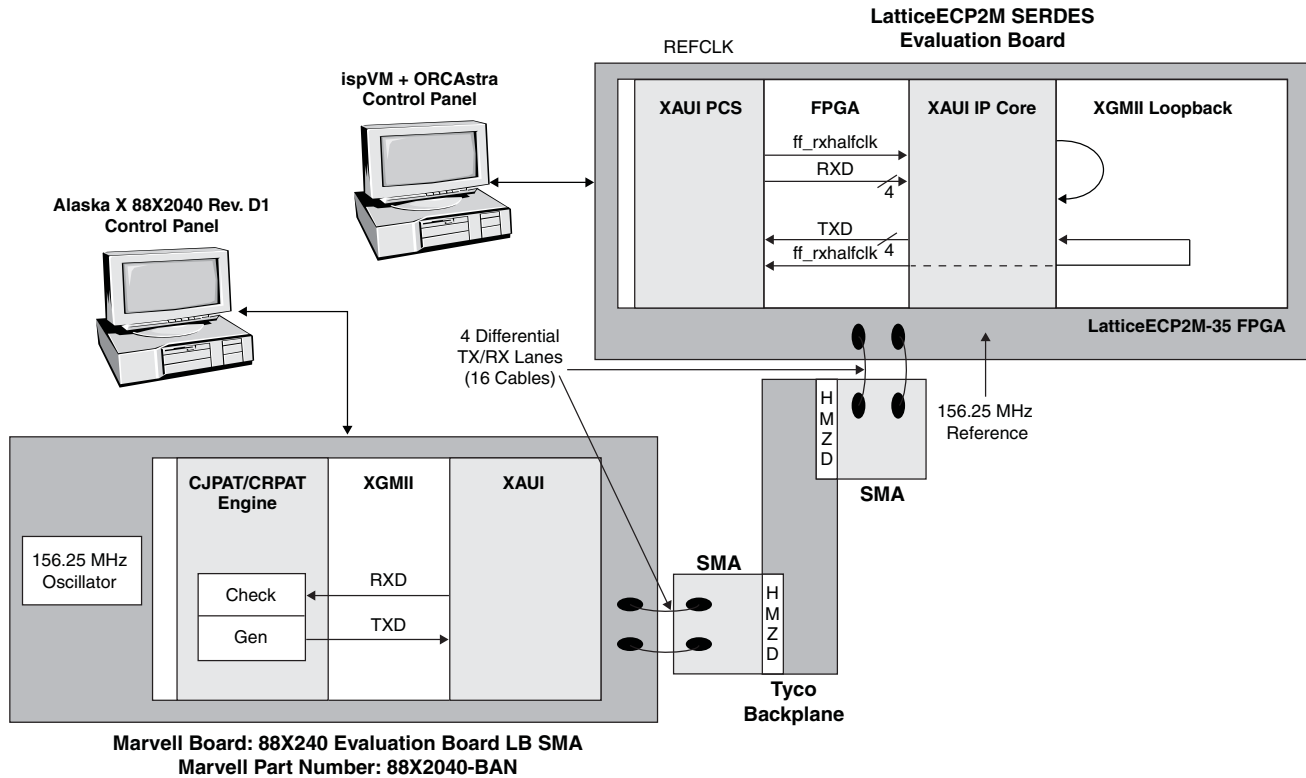




Figure 6. Test Setup Block Diagram



### Test Description

This section describes how each interoperability partner is set up for 10-Gigabit Ethernet physical layer interoperability.

#### Marvell 88X2040 Board

The built-in 156.25 MHz clock oscillator sources the Marvell 88X2040 reference clock for XAUI. The reference clock is multiplied internally by 20 to achieve a 10 Gbps data rate (12.5 Gbps aggregated rate). The Marvell 88X2040 generates and checks full protocol-compliant 10-Gigabit Ethernet (10 Gbps) CJPAT packets at the XGMII interface.

#### LatticeECP2M SERDES Evaluation Board

The external 156.25 MHz clock oscillator sources the LatticeECP2M PCS reference clock for XAUI. The reference clock is multiplied internally by 20 to achieve a 10 Gbps data rate (12.5 Gbps aggregated rate).

In the RX direction, the LatticeECP2M SERDES recovers the packets from the Marvell 88X2040 device and the XAUI IP converts them into XGMII format.

The XGMII loopback logic in the FPGA portion loops the XGMII data back into the TX direction. The LatticeECP2M device then transmits the packets back to the Marvell 88X2040 device.

### Results

The setup ran for about 34 minutes, during which over 1.6 billion packets were transmitted/received error-free. The RX error counters remained at zero.

### Summary

In conclusion, the LatticeECP2M FPGA family is fully XAUI interoperable with the Marvell 88X2040 device.

## Technical Support Assistance

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## Revision History

Date	Version	Change Summary
November 2008	01.0	Initial release.